**國立台北科技大學**

**資訊工程系**

數位邏輯實習報告

Lab 7:Design of Synchronous Sequential Circuits

實作日期:5/1

第21組:

107590026:賴璟霆

107590052:曾華健

Example.3

1. Problem description: output Z = 1 (coincident with the last 1) when any input sequence ending in 101.The system does not reset when a 1 output occurs.

2. Test sequence: Input X = 0 0 1 1 0 1 1 0 1 1 0 1 0 1 0 0 . . .

Output Z = 0 0 0 0 0 1 0 0 1 0 0 1 0 1 0 0

 